

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): John Grebenkemper et al.

Confirmation No.:

Application No.:

Examiner:

Filing Date: April 9, 2004

Group Art Unit:

Title: MULTI-LAYER PRINTED CIRCUIT BOARDS

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e)(1) or (2), and
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **ER616766365US**

Date of Deposit **April 9, 2004**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By Joy C. Ngo

Typed Name: Joy C. Ngo

Respectfully submitted,

John Grebenkemper et al.

By Mary Jo Bertani
Mary Jo Bertani

Attorney/Agent for Applicant(s)
Reg. No. **42,321**

Date: **April 9, 2004**

FORM PTO-1449

ATTY. DOCKET NO.

200312380-1

APPLICATION NO.

CONFIRMATION NO.

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

APPLICANT

Grebekemper, John

FILING DATE

April 9, 2004

GROUP

(Use several sheets if necessary)

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,065,284	11-12-1991	Hernandez	
	1B	5,246,817	09-21-1993	Shipley, Jr.	
	1C	6,444,922 B1	09-03-2003	Kwong	
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	1F				
	1G				
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Eric BENEDICT, PCB DESIGN FOR EMI/EMC COMPLIANCE, July 21, 2000, WEMPEC Seminar, pp 0-48.
	1R	PCBs, EE6471 (KR), November 12, 2002, pp. 259-286.
	1S	PROTO CIRCUIT INC., MULTILAYER PRINTED CIRCUIT BOARD PRIMER.

EXAMINER

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PATENT APPLICATION

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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200312380-1	APPLICATION NO.	CONFIRMATION NO.
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	2Q	Mehdi M. MECHAIK, Ph.D., EFFECTS OF PACKAGE STACKUPS ON MICROPROCESSOR PERFORMANCE, pp. 1-7, Computer Aided Engineering & PCB Design Cisco Systems, San Jose, CA.
	2R	Minjia XU, Yun JI, Todd H. HUBING, Thomas P. VAN DOREN, James L. DREWNIK, DEVELOPMENT OF A CLOSED-FORM EXPRESSION FOR THE INPUT IMPEDANCE OF POWER-GROUND PLANE STRUCTURES, IEEE, 2000, PP. 77-82.
	2S	John B. HOWARD, PCB DESIGN FOR EMC CONTROL CLOCKS AND POWER PLANES, pp. 5B-1 - 5b-13, IEEE Santa Clara Valley EMC '94.

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3Q	Jason CONG, Patrick H. MADDEN, PERFORMANCE DRIVEN MULTI-LAYER GENERAL AREA ROUTING FOR PCB/MCM DESIGNS, pp. 356-361.
3R	Jiunn-Nan HWANG, Tzong-Lin WU, COUPLING OF THE GROUND BOUNCE NOISE TO THE SIGNAL TRACE WITH VIA TRANSITION IN PARTITIONED POWER BUS OF PCB, PP. 733-736, IEEE 2002.
3S	Jun FAN, James L. KNIGHTEN, Norman W. SMITH, Ray ALEXANDER, THE EFFECTS OF SIGNAL LAYER POSITIONS IN MULTI-LAYER PCB DESIGNS, PP. 320-324, IEEE 2002.

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PATENT APPLICATION

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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

4Q	Minjia XU, Todd H. HUBING, Juan CHEN, Thomas P. VAN DOREN, James L. DREWNIAK, Richard E. DUBROFF, POWER-BUS DECOUPLING WITH EMBEDDED CAPACITANCE IN PRINTED CIRCUIT BOARD DESIGN, pp. 22-30, IEEE 2003, Vol. 45, No. 1, February 2003.
4R	Sean MERCER, Ph.D., C. Eng., MINIMIZING RF PCT ELECTROMAGNETIC EMISSIONS, pp. 46, 48, 55-56, www.rfdesign.com, January 1999.
4S	Dallas A. DEAN, SILENCE IS GOLDEN 8 WAYS TO REDUCE NOISE ON YOUR NEXT PCB, pp. 15-17, CMP Media LLC, January 1999.

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